
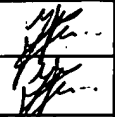
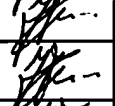
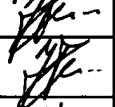
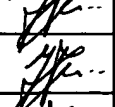
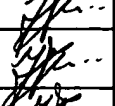
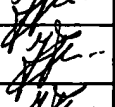
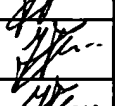
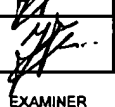
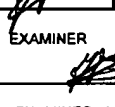
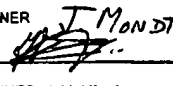


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Form PTO-1039		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2473		SERIAL NO. 10/760,087	
 <p>LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)</p>				APPLICANT Arup Bhattacharyya			
				FILING DATE January 14, 2004		GROUP 2826	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
	AG						
	AH						
	AI						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AJ		King, T. et al., "A Low-Temperature ($\leq 550^\circ\text{C}$) Silicon-Germanium MOS Thin-Film Transistor Technology for Large-Area Electronics", IEDM Tech. Digest, 1991, pp. 567-570.				
	AK		Kuriyama, H. et al., "High Mobility Poly-Si TFT by a New Excimer Laser Annealing Method for Large Area Electronics", IEDM Tech. Digest, 1991, pp. 563-566.				
	AL		Kim, C.H. et al., "A New High-Performance Poly-Si TFT by Simple Excimer Laser Annealing on Selectively Floating a-Si Layer", IEDM Tech. Digest, 2001, pp. 751-754.				
	AM		Hara, A. et al., "High Performance Poly-Si TFTs on a Glass by a Stable Scanning CW Laser Lateral Crystallization", IEDM Tech. Digest, 2001, pp. 747-750.				
	AN		Gu, J. et al., "High Performance Sub-100 nm Si Thin-Film Transistors by Pattern-Controlled Crystallization of Thin Channel Layer and High Temperature Annealing", DRC Conf. Digest, 2002, pp. 49-50.				
	AO		Rim, K. et al., "Characteristics and Device Design of Sub-100 nm Strained Si- and PMOSFETs", 2002 Sympos. on VLSI Tech. Digest of Technical Papers, pp. 98-99.				
	AP		Park, J.S. et al., "Normal Incident SiGe/Si Multiple Quantum Well Infrared Detector", IEDM Tech. Digest, 1991, pp. 749-752.				
	AQ		Saggio, M. et al., "Innovative Localized Lifetime Control in High-Speed IGBT's", IEEE Elec. Dev. Lett., Vol. 18, No. 7, July 1997, pp. 333-335.				
	AR		Lu, N. et al., "A Buried-Trench DRAM Cell Using a Self-Aligned Epitaxy Over Trench Technology", IEDM Tech. Digest, 1988, pp. 588-591.				
EXAMINER 		DATE CONSIDERED 01/28/06					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							